

REMARKS

Claims 12, 22 and 23 have been canceled. Claims 1-11, 13-21 and 24-48 are now pending in this application. Reconsideration of the application is earnestly requested. The Examiner is thanked for the telephone interview of July 19, 2007 in which amendments concerning re-setting the slave component were discussed.

In response to the claim objections, claims 3, 13, 37, 39, 40, 45-48 have been amended as suggested by the Examiner. Claim 12 has not been amended as Applicant believes that the word "transition" is more grammatically correct than the word "transit."

The Office action has allowed claims 4, 14, 15, 19, 20, 24, 25, 29 and 30. Claims 1-3, 11-13, 16, 17, 21-23, 26, 27, 33, 35-37, 39-41 and 43-47 have been rejected under 35 U.S.C. 102(b) as being unpatentable over *Evans et al.* ("Evans," U.S. Pat. No. 6,253,250). Although the Examiner's arguments have been carefully considered, Applicant respectfully traverses this rejection as explained below.

The Present Invention

The instant application points out at page 1, final paragraph, that conventional reset techniques perform a system-wide reset, placing all components into a known state. But, system-wide resets are unnecessarily disruptive. The present invention provides a bus bridge device that handles a reset of components only on a first side of a bus bridge while the second side remains operating freely and without adversely affecting the second side. (See page 3, first paragraph; page 6, lines 15-17; and page 12, lines 14-17.) Further, logic of the bus bridge synchronizes between different clock domains of the different sides so that the side not being reset may transition to an idle state or may be reset subsequently in a safe manner. (Page 6, lines 15-25 and page 12, lines 13-24.)

The Cited Art Distinguished

Claim 1

Claim 1 as amended now requires:

said master component corresponding to a first clock domain and said slave component corresponding to a different second clock domain;

and

synchronizing the reset signal with the first clock domain of the master component such that the master component transitions to an idle state.

The limitations of claim 22 regarding the different clock domains have been incorporated into claim 1. The Office action relies upon the two bus domains of *Evans* and column 1, lines 15-20 as disclosing this limitation. But, there is no disclosure in Figure 2 of *Evans* of the two buses having different clock domains. Further, lines 15-20 mention two independent buses but there is no discussion that these buses have different clock domains.

The limitation of claim 12 regarding synchronization have also been incorporated into claim 1. The Office action relies upon columns 2 and 3 and Figure 2 as disclosing this limitation. But, the Bus2 Exception Monitor 251 of Figure 2 does not synchronize any reset signal with a clock domain on the System 1 side; signal 251 simply provides an indication that an exception has occurred in Bus2. Further, claim 1 requires that the master component transitions to an idle state. There is no disclosure in *Evans* of a component transitioning to an idle state after synchronization. The Office action refers to "stopping data transmission and waiting until no bus exception in Bus2 exists" and cites step 507, but no such phrase or process exists in *Evans*. Step 507 simply discusses determining whether an exception event occurs in Bus2 during transmission of data. Transitioning a component to an idle state is a term of art and is not disclosed simply because an error occurs and a message is marked as lost in transit as indicated in step 509.

For these reasons, it is respectfully requested that the rejection of claim 1 based upon *Evans* be withdrawn.

Claim 11

Claim 11 as amended now requires:

wherein the first side corresponds to a first clock domain and the second side corresponds to a different second clock domain; and

synchronizing the reset signal with the second side of the bus bridge such that a component associated with the second side transitions to an idle state.

As pointed out above with respect to the first and second clock domains being different, *Evans* does not disclose different clock domains. Further, as elaborated upon above, *Evans* likewise does not disclose synchronizing the reset signal with the second side of the bridge such that a component then transitions to an idle state.

For these reasons, it is respectfully requested that the rejection of claim 11 based upon *Evans* be withdrawn.

Claim 21

Claim 21 as amended now requires:

wherein the first side corresponds to a first clock domain and the second side corresponds to a different second clock domain; and

synchronization logic for synchronizing the reset signal with the second clock domain such that the master component and the bus bridge slave interface transition to an idle state.

As discussed above with respect to claim 1, *Evans* does not disclose first and second clock domains that are different. Further, *Evans* likewise does not disclose synchronizing the reset signal with the second clock domain such that the master component transitions to an idle state. Claim 21 further requires that the bus bridge slave interface also transition to an idle state.

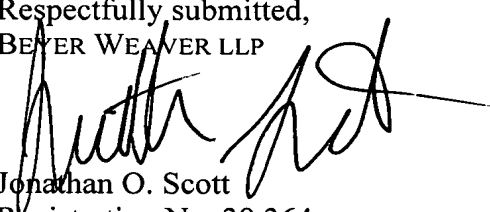
For these reasons, it is respectfully requested that the rejection of claim 21 based upon *Evans* be withdrawn.

Claim 31

Claim 31 is a Beauregard claim that has been amended to require all of the limitations of claim 1, and is submitted to be patentable for the same reasons as discussed above with respect to claim 1.

Reconsideration of this application and issuance of a Notice of Allowance at an early date are respectfully requested. If the Examiner believes a telephone conference would in any way expedite prosecution, please do not hesitate to telephone the undersigned at (612) 252-3330.

Respectfully submitted,
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